



**CVVM**  
**UNIVERSITY**

Aegis: Charutar Vidya Mandal (Estd.1945)

## FACULTY OF ENGINEERING & TECHNOLOGY

Effective from Academic Batch: 2022-23

<b>Programme:</b>	<b>Bachelor of Technology (Computer Engineering)</b>
<b>Semester:</b>	<b>VIII</b>
<b>Course Code:</b>	<b>202047806</b>
<b>Course Title:</b>	<b>High Performance Computing</b>
<b>Course Group:</b>	<b>Professional Elective Course - V</b>

**Course Objectives:** This course provides an overview and fundamentals of the design of high-performance computing (HPC) systems and to understand the means by which to measure, assess and analyze the performance of HPC applications. In addition, students will also learn parallel models of computation.

### Teaching & Examination Scheme:

Contact hours per week			Course Credits	Examination Marks (Maximum / Passing)				
Lecture	Tutorial	Practical		Theory		J/V/P*		Total
				Internal	External	Internal	External	
3	0	2	4	50/18	50/17	25/9	25/9	150/53

\* J: Jury; V: Viva; P: Practical

### Detailed Syllabus:

Sr.	Contents	Hours
1	<b>Introduction to High Performance Computing (HPC):</b> What is HPC? Motivation, Applications, Challenges, Communication (Shared Address Space vs. Message Passing), Parallel Processing Concepts (Quick Overview), Levels of parallelism (instruction, transaction, task, thread, memory, function), Models (SIMD, MIMD, SIMT, SPMD, Dataflow Models, Demand-driven Computation etc), Architectures: N-wide superscalar architectures, multi-core, multi-threaded	07
2	<b>HPC Paradigms:</b> Supercomputing, Cluster Computing, Grid Computing, Cloud Computing, many core Computing, Petascale Systems, Memory Hierarchies, Multi-core Processors: Homogeneous and Heterogeneous, Shared-memory Symmetric Multiprocessors, Vector Computers, Distributed Memory Computers, Application Accelerators / Reconfigurable Computing, Novel computers: Stream, multithreaded, and purpose-built	10



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<b>3</b>	<b>Parallel Algorithms:</b> Parallel models: ideal and real frameworks, Basic Techniques: Balanced Trees, Pointer Jumping, Divide and Conquer, Partitioning, Regular Algorithms: Matrix operations and Linear Algebra, Irregular Algorithms: Lists, Trees, Graphs, Randomization: Parallel Pseudo-Random Number Generators, Sorting, Monte Carlo techniques	<b>10</b>
<b>4</b>	<b>Parallel Programming:</b> Introduction to OpenMP, Parallel constructs, Runtime Library routines, Work-sharing constructs, Introduction to GPU Computing, CUDA Programming Model, CUDA Memory Model, Shared Memory Matrix Multiplication, Additional CUDA API Features	<b>07</b>
<b>5</b>	<b>Message Passing Interface:</b> Overview of MPI, MPI Constructs, OpenMP vs MPI. MPI Introduction. Collective communication. Data grouping for communication. Distributed memory parallel programming with MPI: message passing - introduction to MPI - example - messages and point-to-point communication - collective communication - nonblocking point-to-point communication- virtual topologies - MPI parallelization of Jacobi solver- MPI implementation - performance properties	<b>07</b>
<b>Total</b>		<b>41</b>

#### List of Practicals / Tutorials:

<b>1</b>	Multi-Threaded Hello World parallel programs.
<b>2</b>	Addition of two arrays using parallel programming.
<b>3</b>	Matrix multiplication using parallel programs.
<b>4</b>	Vector multiplication using parallel programs.
<b>5</b>	Configure MPI and test the MPI Interface.
<b>6</b>	Configure OpenMPI interface and perform Hello World Program.
<b>7</b>	Write a program to perform Matrix multiplication using OpenMPI.
<b>8</b>	Write a program to perform Matrix multiplication using Message Passing Interface with size of matrix is 1000.
<b>9</b>	Study of CUDA architecture and Hello World program Using CUDA Programming.
<b>10</b>	Study of various GPU architecture and test performance on different GPU models.
<b>11</b>	Performance analysis of matrix multiplication on different GPU architectures.

#### Reference Books:

<b>1</b>	Georg Hager, Gerhard Wellein, Introduction to High Performance Computing for Scientists and Engineers, Chapman & Hall / CRC Computational Science series, 2011.
<b>2</b>	Victor Eijkhout, Edmond Chow, Robert van de Geijn, Introduction to High Performance Scientific Computing, 2nd edition, revision 2016
<b>3</b>	Introduction to parallel computing, By Ananth Grama (st. al), Addison-Wesley 2nd ed. (2003), ISBN 0201648652
<b>4</b>	Barbara Chapman, Gabriele Jost, Ruud van der Pas, Using OpenMP, MIT Press, 2008.



5	Gropp, Lusk, Skjellum, Using MPI, Using MPI, 2014.
6	Recent publications in IPDPS, PACT, and similar.
7	Wen-Mei W Hwu, David B Kirk, Programming Massively Parallel Processors A Hands-on Approach, Morgan Kaufmann, 3e
8	Rob Farber, CUDA Application Design and Development, Morgan Kaufmann Publishers, 2013
9	Zbigniew J. Czech, Introduction to parallel computing, 2nd edition, Cambridge University Press, 2016

### Supplementary learning Material:

1	NPTEL - <a href="https://nptel.ac.in/courses/106108055">https://nptel.ac.in/courses/106108055</a> <a href="https://onlinecourses.nptel.ac.in/noc20_me61/preview">https://onlinecourses.nptel.ac.in/noc20_me61/preview</a>
2	Coursera - <a href="https://www.coursera.org/learn/introduction-high-performance-computing">https://www.coursera.org/learn/introduction-high-performance-computing</a>

### Pedagogy:

- Direct classroom teaching
- Audio Visual presentations/demonstrations
- Assignments/Quiz
- Continuous assessment
- Interactive methods
- Seminar/Poster Presentation
- Industrial/ Field visits
- Course Projects

### Suggested Specification table with Marks (Theory) (Revised Bloom's Taxonomy):

Distribution of Theory Marks in %						R: Remembering; U: Understanding; A: Applying; N: Analyzing; E: Evaluating; C: Creating
R	U	A	N	E	C	
10%	25%	25%	10%	30%	---	

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

### Course Outcomes (CO):

Sr.	Course Outcome Statements	%weightage
CO-1	To design, formulate, solve, and implement high performance versions of standard single threaded algorithms	20
CO-2	To demonstrate the architectural features in the GPU and MIC hardware accelerators.	30
CO-3	To develop programs to extract maximum performance in a multicore, shared memory execution environment processor.	25
CO-4	To analyze and deploy large scale parallel programs on tightly coupled parallel systems using the message passing paradigm.	25



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<b>Curriculum Revision:</b>	
Version:	2.0
Drafted on (Month-Year):	June-2022
Last Reviewed on (Month-Year):	-
Next Review on (Month-Year):	June-2025