FACULTY OF ENGINEERING & TECHNOLOGY

Effective from Academic Batch: 2022-23

Programme: Bachelor of Technology (Computer Engineering)

Semester: III

Course Code: 202040303

Course Title: Digital Fundamentals

Course Group: Engineering Science

Course Objectives: This course introduces the concepts of digital logic. Digital number systems and basic logic gates are covered. It includes the functionality of logic gates, simplifying Digital Circuits, Boolean Expression, combinational and sequential circuits. Emphasis is placed on providing a foundation for the application of digital logic to use of digital applications such as programmable logic converters.

Teaching & Examination Scheme:

Contact hours per week			Course Credits	Examination Marks (Maximum / Passing)				
Lecture	Tutorial	Practical		Theory		J/V/P*		Total
				Internal	External	Internal	External	
3	0	2	4	50 / 18	50 / 17	20 / 9	20 / 9	150 / 53

* **J**: Jury; **V**: Viva; **P**: Practical

Detailed Syllabus:

Sr.	Contents	Hours
1	**Introduction:** Binary Systems and Logic Circuits, The Advantage of Binary, Number Systems, The Use of Binary in Digital Systems, Logic Gates, Logic Families: Transistor-Transistor Logic(TTL), Emitter-Coupled Logic(ECL), MOSFET Logic, TTL Gates.	04
2	**Boolean Algebra and Logic Gates:** Basic Definition, Axiomatic Definition of Boolean Algebra, Basic Theorem and Properties of Boolean Algebra, Minterms And Maxterms, Logic Operation	05
3	**Simplification of Boolean Functions:** Different types Map method, Sum of Product and Product of sum Simplification, NAND or NOR implementation, Realizing Logic Function with Gates, Combinational Design examples, Don't Care condition, Tabulation method	07

4	**Logic Function Realization with MSI and LSI:** Multiplexer, De-Multiplexer/Decoders, Combinational Logic with Multiplexers and Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder, Digital comparator, Parity checker/generator, Code converters, Standard, Design Problem Using MSI Circuits, ROM, PLA, PAL	**08**
5	**Sequential Logic:** Introduction, Flip-Flops, Triggering of Flip-Flops, Analysis of Clocked Sequential Circuits, Applications of flip-flops, Flip-Flop Excitation Tables, Design Procedure, Design of Counters, Design with State Equations, Shift Register, Applications of Shift Registers	**07**
6	**Introduction to State Machines:** The Need for State Machines, The State Machine, Basic Concepts in State Machine Analysis.	**03**
7	**Synchronous State Machine Design:** Sequential Counters, State Changes Referenced to Clock, Number of State Flip-Flops, Input Forming Logic, Output Forming Logic, Generation of a State Diagram from a Timing Chart, Redundant States, General State Machine Architecture	**06**
8	**Asynchronous State Machines:** The Fundamental-Mode Model, Problems of Asynchronous Circuits Basic Design Principles, An Asynchronous Design Example.	**04**
	Total	**44**

List of Practicals / Tutorials:

1	(a) To study operation of various logic gates AND, OR, NOT, NAND, NOR and EX-OR. (b) To study NAND/NOR as universal gates.
2	(a) Reduce Boolean Expressions to its simplest possible form and implement it using NAND gates. (b) Develop a logic circuit depending on the requirement of the given logic problem and implement the circuit using NAND gates into its simplest form.
3	(a) Design a combinational logic circuit that gives square of the Two-bit number. (b) Design a combinational logic circuit that determines whether given number is prime or non-prime number.
4	(a) Design a BCD to Gray code converter & realize it using various logic gates. (b) Design a BCD to XS – 3 code converter & realize it using various logic gates.
5	Construct Half Adder, Full Adder, Half Subtractor & Full Subtractor and verify the truth-table for each.
6	(a) Realize 8:1 multiplexer using two 4:1 multiplexer. (b) Realize a given logic function using 4:1 Multiplexer and logic gates.
7	(a) Implement a Full Adder circuit using 3:8 Decoder. (b) Compare two four-bit numbers using a 4-bit Magnitude comparator.
8	Design 3-bit Ripple up counter using Master-Slave JK Flip-flops.
9	Design a synchronous counter using any Flip-flops.
10	Using D-Flip-flops set-up following 4-bit Shift Registers. (i) SISO (ii) PIPO (iii) SIPO (iv) PISO

Reference Books:

1	"Digital logic and Computer design", M. M. Mano, Pearson Education India, 2016.
2	"Fundamentals of Digital Circuits", A. Kumar, Prentice Hall India, 2016.
3	"Digital Principles and Applications" Malvino & Leach, McGraw-Hill Education
4	"Modern Digital Electronics", R. P. Jain, McGraw Hill Education, 2009.
5	"Digital Logic & State Machine Design", David J. Comer, Third Indian Edition, Oxford University Press

Supplementary learning Material:	
1	NPTEL website and IITs virtual laboratory
2	MultiSim / LogiSim / Electronic Workbench simulator for practical performance
3	Major Equipment 1. Pattern Generators 2. Logic State Analyzers 3. Digital Storage Oscilloscopes 4. Digital Integrated Circuits Tester. 5. Complete Bread Board Systems, switches and I/O indicators, multimeters, pulse, square wave generators and display facility.

Pedagogy:

- Direct classroom teaching
- Audio Visual presentations/demonstrations
- Assignments/Quiz
- Continuous assessment
- Interactive methods
- Seminar/Poster Presentation
- Industrial/ Field visits
- Course Projects

Suggested Specification table with Marks (Theory) (Revised Bloom's Taxonomy):

Distribution of Theory Marks in %						
R	**U**	**A**	**N**	**E**	**C**	**R**: Remembering; **U**: Understanding; **A**: Applying; **N**: Analyzing; **E**: Evaluating; **C**: Creating
20%	30%	30%	20%	-	-	

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Course Outcomes (CO):

Sr.	Course Outcome Statements	%weightage
CO-1	Solve the given problem using fundamentals of Number systems and Boolean algebra	**20**
CO-2	Analyze working of logic families and logic gates and design the simple circuits using various gates for a given problem	**25**
CO-3	Design and implement Combinational and Sequential logic circuits	**25**
CO-4	Develop a digital logic and apply it to solve real life problems.	**20**
CO-5	Develop a digital logic and apply it to solve real life problems.	**10**

Aegis: Charutar Vidya Mandal (Estd.1945)

Curriculum Revision:	
Version:	2.0
Drafted on (Month-Year):	June-2022
Last Reviewed on (Month-Year):	-
Next Review on (Month-Year):	June-2025